## REMARKS/ARGUMENTS

Applicant responds herein to the Office Action dated May 2, 2007. A Petition for Extension of Time (one month) and the fee therefor are enclosed.

Applicant's attorneys appreciate the Examiner's continued thorough search and examination of the present patent application.

Claims 1-14 are pending in this application. Claims 1-14 have been rejected.

Claims 1-2 and 9-10 have been objected to because allegedly, a "first predefined value" (Claims 1 and 9) and a "second predefined value" (Claims 2 and 10) are two different values not supported by the specifications.

These first and second predefined values refer to different electrical characteristics that are representative of the same threshold. The first predefined value is a threshold for the rate of change of voltage (dv/dt) at one of the main terminals of the power switching transistor. Support for the first predefined value can be found on page 3, lines 25-26, i.e., the last sentence of the first paragraph of the Detailed Description of the Invention section of the specification.

The second predefined value is a threshold for the voltage across the resistor R8, which occurs at essentially the same time and as a result of the dv/dt exceeding the first predefined value. Support for the second predefined value can be found on page 3, lines 27-29, i.e., the first sentence of the second paragraph of the Detailed Description of the Invention section of the specification.

In response to the claim objections, claims 9 and 10 have been amended to refer to "a predefined rate of change value" and "a predefined sensing value" instead of the first and second predefined values, respectively. Further, claim 9, which previously recited "a R-C circuit", has been amended to specifically call out a resistor, a capacitor and a related structure.

New claims 15-19 have been added to more particularly point out and distinctly claim the features of the present invention. New claims 15-19 have been directed to a power supply that comprises a power switching transistor, a storage capacitor, and an overcurrent protection circuit. Thus, new claims 15-19 specifically claim that the overcurrent protection circuit is responsive to the dv/dt across the storage capacitor. No new subject matter was added.

Claims 1-4, 8-11, and 14 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,285,235 to Ichikawa et al. ("Ichikawa"). Reconsideration and withdrawal of

this rejection are respectfully requested.

Claims 5, 6, and 12 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa in view of U.S. Patent No. 5,751,052 to Heminger et al. ("Heminger"). Reconsideration and withdrawal of this rejection are respectfully requested.

Claims 7 and 13 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa in view of U.S. Patent No. 5,818,281 to Ohura et al. ("Ohura"). Reconsideration and withdrawal of this rejection are respectfully requested.

Independent claims 1 and 9 and new independent claim 15, recite an overcurrent protection circuit. In accordance with the present application, the overcurrent protection circuit monitors the voltage across the storage capacitor, which is present at one of the main terminals of the power switching transistor, to detect an overcurrent condition in the storage capacitor. Accordingly, claims 1 recites a sensing circuit for sensing "the rate of change of voltage with respect to time at one of the main electrodes of the power switching transistor". Claim 9 recites a capacitor adapted to generate a current representative of "the rate of change of voltage with respect to time across the storage capacitor." And new claim 15 recites an overcurrent protection circuit operable to sense "the rate of change of voltage with respect to time across the storage capacitor."

Independent claims 1, 9, and 15 respectively recite a protection switch, a protection transistor, and an overcurrent protection circuit that "remove a control signal to the control electrode of the power switching transistor to turn off the power switching transistor" when an overcurrent condition is detected. Specifically, the overcurrent condition is detected if the rate of change exceeds "a predefined value" as in claim 1 or "a predefined rate of change value" as in amended claim 9 and new claim 15.

Ichikawa, at col. 1, lines 20-21, discloses a gate control circuit for an insulated-gate bipolar transistor (IGBT), which is used as the switching element of a power converter. Ichikawa teaches minimizing a delay time between the time when a control signal is provided to turn the IGBT off and the time when the IGBT actually becomes non-conductive. See col. 4, lines 49-50 and Figure 4. Specifically, Ichikawa teaches minimizing the delay time by increasing the amount of current that flows out of a gate of the IGBT to turn the IGBT off quicker. See col. 4, line 66 to col. 5, line 1 and Figure 15.

In Ichikawa, the gate control circuit for controlling the IGBT supplies a positive DC voltage 2A to a gate of the IGBT to conduct a gate current into the gate of the IGBT to turn the IGBT on. Similarly, the gate control circuit supplies a negative DC voltage 2B to the gate of the IGBT to conduct the gate current out of the gate of the IGBT to turn the IGBT off. Since the IGBT operates as the switching element of a power converter, the IGBT switches on and off in a periodic manner as Ichikawa illustrates in Figures 15, 22, and 24.

At col. 11, lines 12-14, Ichikawa describes attempts of the gate control circuit to stop an "outbreak of surge overvoltage" by conducting a "relatively low off gate current" out of the gate of the IGBT to turn the IGBT off. The gate control circuit of Ichikawa continues to switch the IGBT in the periodic manner, but simply decreases the rate at which the IGBT is turned off.

Accordingly, the gate control circuit of Ichikawa does not teach, disclose, or suggest removing a control signal from the gate of the IGBT in response to a high dv/dt condition. Therefore, Ichikawa does not anticipate removing "a control signal to the control electrode of the power switching transistor to turn off the power switching transistor" as recited in independent claims 1, 9, and 15.

Further, Ichikawa discloses detecting a rate of change of the collector-emitter voltage of the IGBT. See col. 10, line 66 to col. 11, line 2 and Figure 23. In the event of a surge overvoltage condition across the collector-emitter junction of an IGBT or other transistor, the transistor should be rendered conductive or more conductive to reduce the voltage across the collector-emitter junction. This is well known to those of ordinary skill in the art. The transistor should not be rendered non-conductive, i.e., the control signal to the control electrode of the transistor should not be completely removed. At col. 11, lines 12-14, Ichikawa teaches scaling back the rate at which the IGBT is turned off to stop an "outbreak of surge overvoltage" across the collector-emitter junction of the IGBT. In contrast, the inventions of claims 1, 9, and 15 include an overcurrent protection circuit to prevent an overcurrent condition in the power switching transistor by monitoring the dv/dt at one of the main terminals of the power switching transistor.

Accordingly, Ichikawa does not teach, disclose, or suggest a sensing circuit for sensing "the rate of change of voltage with respect to time at one of the main electrodes of the power switching transistor", recited in claim 1; a capacitor adapted to generate a current representative

of "the rate of change of voltage with respect to time across the storage capacitor", recited in claim 9; and an overcurrent protection circuit operable to sense "the rate of change of voltage with respect to time across the storage capacitor", recited in claim 15.

Applicants submit that Ichikawa is not an enabling disclosure of a protection circuit for removing a control signal from the control electrode of a power switching transistor in response to the rate of change of voltage with respect to time at one of the main electrodes of the power switching transistor. For the following reasons, Ichikawa should not be relied upon to reject claims 1-4, 8-11 and 14 under 35 U.S.C. §102(b). There is no description in Ichikawa of the voltage rate change detector 20 that detects the rate of change of voltage across the collector-emitter junction of the IGBT or the nature of the signal provided from the voltage rate change detector 20 to the comparator 21.

Further, the figures and specification of Ichikawa are inconsistent. Specifically, Figure 23 shows the voltage $V_C$ measured across the collector-emitter junction of the IGBT and provided as an input to the voltage rate change detector 20. The Ichikawa specification, at col. 10, line 66 to col. 11, line 2, describes detection of "the rate of change of the collector-emitter voltage $V_{CE}$ of the IGBT 1 and outputs the detected value to the comparator 21" by the voltage rate change detector 20. At col. 11, lines 2-3, the Ichikawa specification states that "[t]he comparator 21 compares the detected value with a reference threshold Vref". However, Fig. 24 shows that the voltage $V_C$ (measured across the collector-emitter junction of the IGBT), not the "detected value", i.e., a value representative of the dv/dt, is compared to the reference threshold Vref. Applicants submit that one of ordinary skill in the art would have difficulty determining the teachings of Ichikawa.

Thus, because Ichikawa does not anticipate each and every element of independent claims 1 and 9 and new independent claim 15, Ichikawa does not anticipate these claims.

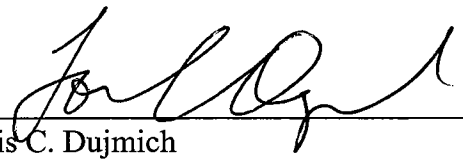
The Examiner did not use Heminger and Ohura in rejecting the independent claims.

Claims 2-8, 9-14, and new claims 16-19 depend directly or indirectly from above discussed independent claims and are, therefore, allowable for the same reasons, as well as because of the combination of features in those claims with the features set forth in the respective independent claims.

In view of the above, it is submitted that all claims in this application are now in condition for allowance, prompt notification of which is requested.

THIS CORRESPONDENCE IS BEING SUBMITTED ELECTRONICALLY THROUGH THE PATENT AND TRADEMARK OFFICE EFS FILING SYSTEM ON August 16, 2007.

Respectfully submitted,



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